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EXAMINER	
XIAO, KE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/015,679	HAM, YONG SUNG	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 4 and 6-14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hanano (US 6,535,194).

Regarding **Claim 1**, Hanano teaches a liquid crystal display device (Hanano, Fig. 1), comprising:

a liquid crystal display panel having pixels for displaying an image (Hanano, Fig. 1 elements image signal, 11 and 1b); and

a light shutter on the liquid crystal display panel operable to transmit and shut off light emitted from the liquid crystal display panel during every field period (Hanano, Figs. 1, 4a-4f element 12 and 2, Col. 12 line 49 to Col. 13 line 6),

wherein every field period is initiated upon a first transition of a gate signal from a low voltage signal to a high voltage signal to apply image data to the pixels and is terminated upon a next transition of the gate signal from a low voltage signal to a high voltage signal to apply image data to the pixels, and wherein every field period

corresponds to only one image data value (Hanano, Fig. 5a Even and Odd halves make up a single frame image which is a single image data value),

and wherein the light shutter is opened at a first transition of the gate signal such that the transmittance of the light shutter is substantially zero before opening (Hanano, Fig. 5a before opening of the shutter the transmittance is clearly zero) and closed after the first transition of the gate signal and before the next transition of the gate signal per every frame period for each pixel such that the transmittance of the light shutter is substantially zero after closing (Hanano, Fig. 5a, first transition at beginning of frame opens shutter, and before the second transition at the next frame the shutter is closed for the odd field after td and the transmittance is clearly zero).

Regarding **Claim 7**, Hanano teaches an apparatus for driving a liquid crystal display (Hanano, Fig. 1) comprising:

a liquid crystal display panel having a pixel for displaying an image (Hanano, Fig. 1 elements image signal, 11 and 1b);

a light shutter on the liquid crystal display panel operable to transmit and shut off light emitted form the liquid crystal display panel during every field period (Hanano, Figs. 1, 4a-4f element 12 and 2, Col. 12 line 49 to Col. 13 line 6),

a controller generating a shutter control signal to open or close the light shutter (Hanano, Fig. 1 element 11 and Sync Signal); and

a light shutter driver responding to the shutter control signal to drive the light shutter (Hanano, Fig. 1 element 12),

wherein every field period is initiated upon a first transition of a gate signal from a low voltage to a high voltage signal to apply image data to the pixel and is terminated upon a next transition of the gate signal from a low voltage signal to a high voltage signal to apply image data to the pixels, and

wherein every field period corresponds to only one image data value (Hanano, Fig. 5a Even and Odd halves make up a single frame image which is a single image data value),

and wherein the light shutter is opened at a first transition of the gate signal such that the transmittance of the light shutter is substantially zero before opening (Hanano, Fig. 5a before opening of the shutter the transmittance is clearly zero) and closed after the first transition of the gate signal and before the next transistor of the gate signal per every frame period for each pixel such that the transmittance of the light shutter is substantially zero after closing (Hanano, Fig. 5a, first transition at beginning of frame opens shutter, and before the second transition at the next frame the shutter is closed for the odd field after td).

Regarding independent **Claim 13**, Hanano teaches a method of driving a liquid crystal display having a light shutter on the liquid crystal display panel (Hanano, Fig. 1), comprising:

supplying a video data to a liquid crystal display panel having a pixel for displaying an image according to a gate signal (Hanano, Figs. 1 and 5a elements image signal, 11 and 1b and gate control for shutters); and

opening the light shutter at a first transition of the gate signal from a low voltage signal to a high voltage signal such that the transmittance of the light shutter is substantially zero before opening (Hanano, Fig. 5a Even and Odd halves make up a single frame image which is a single image data value and the shutter is clearly closed/zero transmittance before it is opened); and

and closing the light shutter after the first transition of the gate signal and before a next transition of the gate signal from a low voltage signal to a high voltage signal per every frame period for each pixel such that the transmittance of light shutter is substantially zero after closing (Hanano, Fig. 5a, first transition at beginning of frame opens shutter, and before the second transition at the next frame the shutter is closed for the odd field after td).

Regarding **Claim 3**, Hanano further teaches that the light shutter has a polarizer to transmit a linearly polarized light (Hanano, Figs. 1 and 24a-24b element 6).

Regarding **Claim 4**, Hanano further teaches that the liquid crystal display panel and the light shutter are bonded with each other and have a polarizer there between (Hanano, Figs. 1 and 24a-24b element 6).

Regarding **Claim 6**, Hanano further teaches that the LCD comprises a backlight irradiating a light toward the liquid crystal display panel (Hanano, Fig. 1 element 1a).

Regarding **Claim 8**, Hanano further teaches that the shutter control signal has an inverse polarity after video data having an inverse polarity are applied to the liquid crystal display panel (Hanano, Figs. 4c and 4d).

Regarding **Claim 9**, Hanano further teaches that the shutter control signal is a pulse signal having a first logical value turning on the light shutter and a second logical value turning off the light shutter (Hanano, Fig. 4f).

Regarding **Claim 10**, Hanano inherently teaches:

a data driver connected to a plurality of data lines of the liquid crystal display panel to apply video data to the data lines (Hanano, Figs. 9, 10a-10e, element 42, Col. 15 lines 35-52), and

a gate driver connected to a plurality of gate lines of the liquid crystal display panel to apply a scanning signal to the gate lines (Hanano, Figs. 9, 10a-10e, element 42, Col. 15 lines 35-52).

To elaborate, data and gate drivers are inherently required to operate the display device as described by Hanano. Specifically, scan data and timing pulses shown in Fig. 10 are generated by the gate and data drivers in order for the display to be able to show an image as described.

Regarding **Claim 11**, Hanano inherently teaches that the data driver is connected to the controller that generates the video data and a dot clock and controls the data driver, and the gate driver is connected to the controller that generates a gate start pulse allowing the scanning signal to be sequentially generated and controls the gate driver (Hanano, Fig. 9, 10a-10e).

To elaborate, all the components of the image display driver are connected either directly or indirectly with one another, and the dot clock shown in Fig. 10b controls the output of image data to the display, the gate driver generates the gate start pulse

allowing the scanning signal to be sequentially generated and controls the gate driver as shown in Fig. 10a.

Regarding **Claim 12**, Hanano further teaches that the shutter control signal has a first logical value in an initial field interval when video data are applied to the liquid crystal display panel and has a second logical value in a time interval when the video data are maintained at the liquid crystal display panel (Hanano, Figs. 4a-4g, 12, Col. 11 lines 39-41, Col 16 lines 1-7).

Regarding **Claim 14**, Hanano further teaches applying a shutter control signal having a first logical value in an initial field interval when the video are applied to the liquid crystal display panel, and a second logical value in a time interval when the video data are maintained at the liquid crystal display panel (Hanano, Figs. 4a-4g, 12, Col. 11 lines 39-41, Col 16 lines 1-7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanano (US 6,535,194) in view of Matsumoto (US 4,097,128).

Regarding **Claims 2 and 5**, Hanano fails to teach that the light shutter includes;

a liquid crystal between two glass substrates, a plurality of electrodes on the two glass substrates to drive the liquid crystal, and that the liquid crystal display panel and the light shutter are bonded to a single glass substrate.

Matsumoto teaches a liquid crystal display device with a light shutter and a liquid crystal display device, wherein the light shutter includes

a liquid crystal between two glass substrates (Matsumoto, Fig. 3 elements 33 LC 31 and 35 Glass);

a plurality of electrodes on the two glass substrates to drive the liquid crystal (Matsumoto, Fig. 3 elements 32 and 34); and

that the liquid crystal display panel and the light shutter are bonded to a single glass substrate (Matsumoto, Fig. 3 element 35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the structure as taught by Matsumoto in the display device of Hanano in order to allow more independent control of both the liquid crystal display panel as well as the shutter layer.

Response to Arguments

Applicant's arguments filed October 14th 2008 have been fully considered but they are not persuasive.

Regarding independent **Claims 1, 7 and 13**, the applicant argues the following points:

a) Hanano fails to teach "only one image data value" as claimed.

The examiner respectfully disagrees. In this case "only one image data value" *must* be broadly interpreted in light of the applicant's specification. Only one image data value can mean a plurality of different things in a plurality of different contexts. For example an extremely literal interpretation would mean a single bit of image data, which would essentially contradict the applicant's specification, therefore the examiner took "only one image data value" to mean the image data required to display one full frame which is exactly what Hanano teaches.

b) Hanano fails to teach the newly added limitations where "the transmittance of the light shutter is substantially zero before opening" and "the transmittance of the light shutter is substantially zero after closing".

The examiner respectfully disagrees. Hanano clearly teaches that the transmittance of the light shutter is zero both before opening and closing (Fig. 5 before even field it is zero, after even field it is also zero). The applicant's arguments are based on the fact that Hanano fails to teach that the transmittance is substantially zero *immediately* before opening and after closing of the light shutter, however such an assertion would also be impossible for the applicant's invention to achieve since there must *inherently* be a transition period between opening and closing of the light shutter. Even if this weren't a concern, the claims also recite only "before" and "after" meaning anytime before and anytime after, since there is no other mention of time frame within the claimed limitation.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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